

## REMARKS

Claims 3, 4, 9, and 12-14 are pending in the above-identified application.

### Objections

Claim 4 stands objected to for informalities. Claim 4 has been amended to depend upon claim 3 as suggested by the Examiner to overcome the objection. No new matter has been added.

Reconsideration and withdrawal of the objection are respectfully requested.

### Rejection under 35 U.S.C. §112

Claim 4 stands rejected under 35 U.S.C. §112, second paragraph for insufficient antecedent basis. Claim 4 has been amended to correct for antecedent basis. Reconsideration and withdrawal of the rejection are respectfully requested.

### Rejection under 35 U.S.C. §103(a)

Claims 3, 4, 9, 12, 13 and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 5,894,146 issued to Pio et al. (herein "Pio") in view of U.S. Pat. No. 5,851,886 issued to Peng (herein "Peng"). The rejections of claims 3, 4, 9, 12, 13 and 14 are respectfully traversed in view of the following remarks.

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation to modify the reference, there must be a reasonable expectation of success, and the prior art references when combined must teach or suggest all of the claim limitations (see MPEP 2142). It is respectfully submitted that the combined references do not teach or suggest all of the claim limitations. It is further respectfully submitted that there is no

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motivation to modify or combine the teachings of Peng with those of Pio. Thus, the Examiner is using impermissible hindsight to try to reconstruct the claimed invention.

Claims 3 and 9 recite, in part, "*channel region having a non-uniform concentration of dopant*" and further recite "*said non-uniform concentration comprises a lateral concentration distribution along the length of the channel*". There is no motivation to provide "*channel region having a non-uniform concentration of dopant*" and "*said non-uniform concentration comprises a lateral concentration distribution along the length of the channel*" for Pio because the "*lateral concentration distribution along the length of the channel*" in the devices of Peng is provided for purposes that are inapplicable to the devices of Pio. Peng teaches structures for "*decreasing threshold voltage ( $V_t$ ) [and] sensitivity to variation in gate length ( $L_g$ ) caused by manufacturing techniques*" (Peng, column 1, lines 61-64). Neither of these purported advantages applies to the EEPROMs of Pio which use stacked (floating) gate transistors and high voltages (Pio, column 4, lines 38-44), in contrast with the low voltage, single gate device of Peng.

For at least the above reasons, and since there is no motivation to modify the teachings of Pio with the teachings of Peng, the Examiner has not established *prima facie* obviousness for claims 3 or 9. For at least this reason, claims 3 and 9 patentably distinguishable over the cited references, and allowance of claims 3 and 9 under 35 U.S.C. §103(a) is respectfully requested.

Furthermore, even assuming, for the sake of argument only, that the teachings of Peng could be combined with those of Pio, it is further respectfully submitted that the combined prior art references do not teach or suggest all of the limitations of claims 3 or 9. It is further respectfully submitted that Pio, either alone or in combination with Peng, is not sufficient to render any of independent claims 3 or 9 obvious under 35 U.S.C. §103(a).

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For example, claims 3 and 9 recite, in part, "*channel region having a non-uniform concentration of dopant*" and further recite "*wherein said non-uniform concentration comprises a retrograde concentration distribution in the direction from the surface of the substrate*". But there is nothing in Pio or Peng to disclose, teach or render obvious these limitations. Indeed Pio and Peng are each completely silent as to retrograde dopant distributions.

Therefore, for at least this additional reason, the Examiner has not established *prima facie* obviousness for claims 3 or 9. For at least this reason, claims 3 and 9 are patentably distinguishable over the cited references, alone and in combination, and allowance of claims 3 and 9 under 35 U.S.C. §103(a) is respectfully requested.

Claim 4 depends upon claim 3 and is thus allowable for at least the same reasons as claim 3.

Claims 12, 13 and 14 depend, directly or indirectly, upon claim 9 and are thus allowable for at least the same reasons as claim 9.

With regard to the Examiner's assertion that claims 4 and 12 are unpatentable product-by-process claims for an old or obvious product even if produced by a new method, it is respectfully submitted that none of the cited art discloses, teaches or renders obvious the claimed non-uniform channel doping in both vertical and horizontal directions in combination with the other claim limitations. Thus, products created in conformity with the present invention are novel structures. Indeed, as recited in the application, a purpose of creating such a structure is "*avoid effects such as punch-through*" while also "[to] maintain a sufficiently high read current in a floating gate MOSFET" and consistent with "*achiev[ing] higher density ...at a low sub-micro level*" (see specification page 1, lines 24-25, 31-32 and

20-21 respectively). Thus, there has been a clear showing of both novelty and utility to the inventions of claims 4 and 12. Thus, claims 4 and 12 are allowable under the cited case law relating to product-by-process inventions.

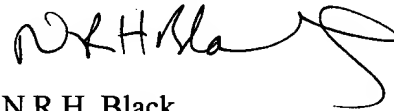
### CONCLUSION

For the above reasons, Applicants believe all the pending and elected claims 3, 4, 9, 12, 13 and 14 are now in condition for allowance and a notice of allowance is respectfully requested.

If the Examiner has any questions regarding the application, the Examiner is invited to call the undersigned at (415) 217 6000.

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Respectfully submitted,



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Marked-Up Version Of The Amended Claim

4. The memory array of claim [1] 3 wherein
- the non-uniform concentration is formed by a tilted ion implantation utilizing
- as a mask a gate structure of each floating gate [NMOS] transistor.

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